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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/658,732	09/11/2000	Makoto Inai	P/1071-1118	4527

7590 05/18/2004

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EXAMINER	
BAUMEISTER, BRADLEY W	
ART UNIT	**PAPER NUMBER**
2815	

DATE MAILED: 05/18/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/658,732	INAI ET AL.	
	Examiner	Art Unit	
	B. William Baumeister	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *3/8/2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-10 and 12-15* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10 and 12-15* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *3/8/2004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

2. Claims 1-10 and 12-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sawada et al., "A Super Low-Noise AlGaAs/InGaAs/GaAs DC-HFET with 0.15 micron Gate-Length" [Sawada] in view of Enoki, "Delay Time Analysis for 0.4- to 5-micron-Gate InAlAs-InGaAs HEMT's" [Enoki].

a. Sawada discloses a DC-HFET having a doped channel composed of n-InGaAs; a doped barrier (or semiconductor structure) composed of n-AlGaAs (a material having a lower electron-affinity than that of the channel); and a doped contact composed of n-GaAs. An ohmic electrode is formed on the GaAs contact layer and a Schottky electrode is formed on the barrier layer semiconductor structure. The doped AlGaAs barrier forms isotype heterojunctions with the InGaAs channel and the GaAs contact layers. Sawada further teaches that various structural- and doping-configuration modifications for the barrier layer may be employed with the DC-HFET to further optimize or adjust various conventionally-understood device parameters. For example, compare the embodiment of FIG 1 wherein an undoped barrier exists between the n-doped InGaAs channel and the n-GaAs cap with the embodiment of FIG 6 wherein the barrier layer is undoped beneath the gate and doped beneath the source and drain, thereby maintaining an enhanced gate Schottky barrier while reducing the series resistance between the channel and the cap layers (page 355, col. 1, section 4, first paragraph).

Sawada does not anticipate the claims because it does not teach the further inclusion of an undoped layer/region disposed between the doped top and the bottom regions of the AlGaAs barrier layer, nor that the gate makes Schottky contact particularly to this undoped layer region (claim 14).

b. Enoki teaches III-As-based HEMT HFETs that comprise an n-InGaAs channel; an InAlAs "semiconductor structure" comprised successively of an n-doped, undoped, and n-doped layer; an n+ InGaAs contact layer for connection of ohmic electrodes; and a Schottky gate that contacts the middle, undoped layer of the "semiconductor structure." (See e.g., FIG 1) Enoki specifically states that "the undoped InAlAs layer between two highly doped InAlAs layers is to enhance the Schottky barrier of the gate metal. The upper n+-InAlAs layer is designed to reduce the source and drain series resistance." (Page 502, col. 1, section II)

c. It would have been obvious to one of ordinary skill in the art at the time of the invention to have modified the Sawada n-AlGaAs barrier layer by providing an additional undoped layer between the top and bottom portions (or restated, by temporarily stopping and restarting the dopant supply during the growth of the barrier layer) for the purpose of enhancing the Schottky barrier of the gate while simultaneously providing a source/drain series resistance that is reduced relative to if the upper portion of the barrier was undoped, as taught by Enoki; and also for the purpose of providing both of these advantages while simultaneously obviating the need for the additional masking steps that would be required to achieve the structure of Sawada's FIG. 6 embodiment wherein the dopant implant is provided for only the S/D regions.

d. Regarding claims 3, 5 and 7, while Sawada discloses a DC-HFET having a heavily doped channel, barrier and cap layer, wherein the respective junctions are all iso-type

heterojunctions, Sawada does not teach the limitations of claim 3 which recites that the layers of the channel/barrier junction and the barrier/contact junction are all doped 1E18. Rather, Sawada--while also disclosing that these layers are all heavily doped to the same order of magnitude--sets forth specific, slightly higher doping concentrations for the channel, barrier and contact layers of 2.5E18, 1.5E18 and 3E18, respectively.

Nonetheless, it would have been obvious to one of ordinary skill in the art at the time of the invention to have modified the doping concentrations to the particular doping levels set forth in claim 3 because the doping levels of the Sawada layers are all heavily doped to the same order of magnitude as that claimed, and such minor changes to the doping levels would not produce any unexpected results, but rather constitute an optimization of results readily obtainable through routine experimentation: more specifically, lowering the barrier doping concentration from 1.5E18 to 1E18 would merely produce the expected results of proportionally increasing the gate-barrier layer Schottky barrier and slightly increasing the source/drain resistance; decreasing the channel doping from 3E18 to 1E18 would slightly reduce both the channel/barrier heterojunction barrier and the carrier-impurity scattering in the channel; and reducing the contact doping from 3E18 to 1E18 would proportionally increase the source and drain resistances.

Response to Arguments

3. Applicant's arguments filed 3/8/2004 have been fully considered but they are not persuasive.

a. Applicant has requested that the examiner provide evidence to support the latter's conclusion that one of ordinary skill in the art would have expected that the enhanced gate Schottky barrier achieved in Enoki with a doping layer with more than twice the doping of the doping layer of Sawada could be achieved in the doping layer of Sawada.

However, the issue is not whether heavily doping portions of the barrier to 1.5e18 vs. 4e18 will enhance the Schottky barrier for the gate. In fact, the more heavily n-doped a barrier layer is, the closer the Fermi energy level is to the conduction band energy level, or restated, the lower the gate Schottky barrier is. Rather, it is the inclusion of the undoped region or sublayer within the heavily doped barrier layer that raises the gate Schottky barrier. By definition, the undoped sublayer has an impurity doping concentration that is on the order of about 1e15-1e16 atoms/cm^3 or lower, at least two to three orders of magnitude lower than the sandwiching layers that are doped on the order of 10^18 atoms/cm^3 for both Sawada and Enoki. Enoki teaches this doping structure, and Sawada evidences that the ordinarily skilled artisan would have expected these well-understood, conventional semiconductor principles to also be applicable in an AlGaAs system as well as an InAlAs system: see e.g., FIG. 6 wherein the GaAs barrier layer possesses source/drain regions that are heavily doped to decrease the Schottky barrier to the source/drain regions (or make the S/D contacts more ohmic, or decrease the S/D resistance), and also possesses an undoped region under the gate (a region doped at least a few orders of magnitude lower than the S/D regions) for providing an increased gate Schottky barrier relative to if the gate region were also doped.

b. Applicant next argues:

> Second, in paragraph no. 4 on page 5 of the Advisory Action the Examiner alleged, "Enoki was relied upon for its broader teaching that within a FET of given

material system, the doped-barrier layer thereof may be further provided with an undoped region for influencing the Schottky barrier height..." The Examiner has indicated that he is relying upon the first paragraph of Enoki et al. under the section "II. Device Structures and Performances" to support this allegation. This portion of Enoki et al. discloses, [t]he doping density for n+-InAlAs was 4×10^{18} cm^{-3}. The undoped InAlAs layer between two highly doped InAlAs layers is to enhance the Schottky barrier of the gate metal" (emphasis added). The Examiner has completely failed to explain how this specific teaching of Enoki et al. that an undoped layer of InAlAs between two doped layers of n+-InAlAs with doping density of $4x10^{18}$ cm^{-3} reduces the Schottky barrier of the gate metal supports the general allegation that any undoped layer between any two doped layers having any doping density reduces the Schottky barrier of the gate metal.

First, Applicant misunderstands the Examiner's position. As explained by Enoki, the further inclusion of an undoped InAlAs layer between two heavily doped n-type InAlAs layers will increase—not decrease—the Schottky barrier relative to if the undoped layer were not present.

Second, the examiner did not make "the general allegation that **any** undoped layer between **any** two doped layers having **any** doping density reduces [sic: increases] the Schottky barrier of the gate metal." Rather, as was explained previously and hereinabove, the examiner's assertion was, and is, that including an undoped layer between sandwiching heavily doped barrier layers and in contact with the gate metal will increase the gate Schottky barrier relative to if the undoped layer was not present, at least when (1) the undoped layer is composed of the same base composition as the doped barrier layers (i.e., the doped/undoped/doped barrier layers form two homojunctions); and (2) the doped barrier layers are n-doped on the order of 10^18 (i.e., at least a few orders of magnitude greater than the undoped layer), in the manner taught by Enoki. The "allegation" that this effect also applies to semiconductor material systems other than InAlAs is based on the well-understood physics principles that in an undoped III-V semiconductor, the Fermi energy level is positioned approximately midway between the

conduction and valence bands, and that n-doping III-V semiconductor materials shifts the Fermi energy level towards the conduction band.

c. Applicant also argues (third argument) that because the inclusion of an undoped layer will increase the resistance of the device, such a modification to Sawada would render this prior art invention being modified unsatisfactory for its intended purpose, and as such there is no suggestion or motivation to make the propped modification. This argument is not persuasive.

Enoki teaches that the inclusion of an undoped layer in the middle of the barrier—to which the gate is in direct, Schottky contact—enhances (or increases) the Schottky barrier. Enoki also teaches that the further inclusion of the upper highly n-doped barrier layer—that forms a junction with the superposed highly n-doped, lower bandgap, InGaAs contact layer—reduces the series resistance, at least sufficiently to allow the HFET to operate as intended. As such, the further inclusion of an undoped layer composed of the same material as the rest of Sawada's barrier layer would not cause the barrier to possess unsatisfactorily high resistance because the additional presence of the upper, highly n-doped region of the AlGaAs barrier layer that forms a junction with the GaAs S/D contact layers in Sawada would sufficiently reduce the S/D series resistance to allow the Sawada HFET to operate as intended, as taught by Enoki.

Contact Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to B. William Baumeister whose phone number is (571) 272-1722. The examiner can normally be reached on M-F 9-6.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on (571) 272-1664. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

BRADLEY BAUMEISTER
PRIMARY EXAMINER

B. William Baumeister
Primary Examiner
Art Unit 2815

May 14, 2004